

BACK SIDE COATING OF SEMICONDUCTOR WAFERS

FIELD OF THE INVENTION

The present invention is related in general to the field of electronic systems and semiconductor devices, and more specifically to materials and fabrication methods of back side coating of semiconductor wafers and the application in flip-chip assembly.

DESCRIPTION OF THE RELATED ART

The large majority of semiconductor devices are manufactured by attaching the passive surface of an integrated circuit (I/C) chip to a metallic leadframe, bonding the chip input/output (I/O) pads on the active surface to the leadframe leads with connecting wires, and encapsulating the assembly, including the sensitive wires, in molding compound. The leadframe for semiconductor devices and the transfer molding technique have been invented by U.S. Patents # 3,716,764, issued on 2/13/1973 (Birchler et al., "Process for Encapsulating Electronic Components in Plastic") and # 4,043,027, issued on 8/23/1977 (Birchler et al., "Process for Encapsulating Electronic Components in Plastic").

On the other hand, semiconductor chips assembled "face-down" (active surface down) onto a substrate using solder balls, do not necessarily need a protective encapsulation, since there are no sensitive connecting wires to be protected. However, other reliability risks related to this "flip-chip" assembly as well as the

requirements for special I/O pad metallizations, have been described in a series of detailed publications by the International Business Machines Corporation in 1969 (IBM J. Res. Develop., Vol. 13, pp. 226 - 296): P. A. Totta et al.,
5 SLT Device Metallurgy and its Monolithic Extension, L. F. Miller, Controlled Collapse Reflow Chip Joining, L.S. Goldmann, Geometric Optimization of Controlled Collapse Interconnections, K. C. Norris et al., Reliability of Controlled Collapse Interconnections, S. Oktay, Parametric
10 Study of Temperature Profiles in Chips Joined by Controlled Collapse Techniques, B. S. Berry et al., Studies of the SLT Chip Terminal Metallurgy.

With the increasing demand to reduce the size and thickness of the semiconductor devices, current industry
15 trend is to use the bare silicon itself as the package. These "chip-size" packages (the extreme case of a "chip-scale" package) are usually bumped on the I/O pads to provide interconnections with the outside part (usually a printed circuit board). To keep the overall device
20 thickness as low as possible, these devices are generally not molded or encapsulated in the traditional sense. However, in order to achieve some level of protection, liquid or viscous compounds have been applied to the exposed surfaces by screen printing or spinning. For these
25 processes, specialized equipment and controls are needed to achieve sufficient product control, which, in turn, results in substantial equipment and process cost.

When unprotected devices are mounted on a printed circuit board (PCB) with the active chip surface down
30 (flip-chip mounting), the bare passive chip surface of the device is exposed to the elements. Since semiconductor materials such as silicon are photo-sensitive, the exposure

to ambient light of the passive chip surface can produce undesirable electrical noise, especially when the chip itself is thin.

An urgent need has, therefore, arisen for a coherent, low-cost method of protecting passive surface of the semiconductor chip from the ambient light. The challenge of cost reduction implies a drive for minimizing the number of process steps, and the application of standardized materials and process conditions wherever possible. The device structure should further enhance mechanical stability and high reliability. The fabrication method should be simple and suitable for batch processing, yet flexible enough for different semiconductor product families and a wide spectrum of design and process variations. Preferably, these innovations should be accomplished with minimum extension of product cycle time, and using installed equipment, so that no investment in new manufacturing machines is needed.

SUMMARY OF THE INVENTION

The present invention describes a semiconductor device comprising a semiconductor chip having an active and a passive surface; the active surface includes an integrated circuit (I/C) and input/output (I/O) pads suitable for metallurgical contacts. Further, the device has a protective plastic film of controlled and uniform thickness selectively attached to the passive surface. The film is suitable to absorb light of visible and ultraviolet wavelengths, to remain insensitive to moisture absorption, and to exert thermomechanical stress on the chip such that this stress at least partially neutralizes the stress exerted by an outside part after chip assembly.

The plastic film is selected from a group of electrically insulating materials consisting of polyimide, epoxy resin, and silicone, and the film further includes hardener, tackyfier, and fillers.

The film thickness preferably ranges from 20 to 60 μm , the light absorption is at least 96 %, and the neutralizing stress is provided by a film coefficient of thermal expansion (CTE, about 18 to 45 $\text{ppm}/^\circ\text{C}$) approximately matching the CTE of the outside part, such as a printed wiring board. After curing the film has an adhesion strength of about 400 kg/cm^2 and a modulus of about 16 GPa.

The film is rolled onto the passive surface of the whole semiconductor wafer and cured at elevated temperatures, preferably about 150 $^\circ\text{C}$, for a length of time of about 1 hr. After film hardening, the wafer sawing process is applied to semiconductor and film material concurrently in order to singulate the individual chips.

The technical advances represented by the invention,
as well as the aspects thereof, will become apparent from
the following description of the preferred embodiments of
the invention, when considered in conjunction with the
5 accompanying drawings and the novel features set forth in
the appended claims.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic cross section of a semiconductor chip having a protective plastic film attached to the passive chip surface according to the invention.

FIG. 2 is an example of light absorption data (in %) as a function of light wavelength (in nm); the data are measured for the plastic film LE-5000X manufactured by the company Lntec, Japan.

FIG. 3 is an example of light absorption data (in %) as a function of light wavelength (in nm); the data are measured for the plastic film NEX-930L manufactured by the company NSC, Nippon Steel Chemical, Japan.

FIG. 4A is a schematic top view of the passive surface of a semiconductor wafer.

FIG. 4B is a schematic top view of the light-absorbing plastic film as used by the invention.

FIG. 5A is a schematic perspective view of a roll of plastic film with its two disposable cover sheets as employed by the invention.

FIG. 5B is a schematic cross section of the plastic film and its two cover sheets before disposal of the cover sheets.

FIG. 6 is a schematic top view of the semiconductor wafer after the process step of attaching the light-absorbing plastic film.

FIG. 7 is a schematic representation of the process step of curing the film-covered wafer in a curing oven.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is related to U.S. Patent Application # TI-33535, filed on 11/ . ./2001 (Zuniga-Ortiz
5 et al., "Bumpless Wafer-Scale Device and Board Assembly"), which is herewith incorporated by reference.

The schematic cross section of FIG. 1 illustrates an embodiment of the present invention, which summarizes the innovative features. A semiconductor device, generally
10 designated 100, comprises a semiconductor chip 101, which has an active surface 101a including an integrated circuit (I/C) and a passive surface 101b. The integrated circuit includes input/output (I/O) pads 102, which are suitable for metallurgical contacts 102a.

15 While the semiconductor chip 101 is commonly silicon, the invention is limited to silicon. The semiconductor material may also be silicon germanium, gallium arsenide, or any other semiconductor material used in I/C fabrication.

20 The I/C has a metallization pattern 103 including the plurality of contact pads 102. The chip metallization 103 may consist of aluminum, copper, or alloys thereof. The IC surface is protected by a dielectric protective overcoat 104, usually silicon nitride of about 1 μ m
25 thickness. As FIG. 1 illustrates, the photoresist window defining contact pad 102b has been opened through the protective overcoat 104.

30 When layer 103 is aluminum or aluminum alloyed with 0.5 to 2 % copper and/or 0.5 to 1 % silicon (layer 0.4 to 1.5 μ m thick), the contact pad exhibits under the aluminum frequently a thin layer (4 to 20 nm thick) of titanium, titanium nitride, titanium tungsten, tantalum, tantalum

nitride, tantalum silicon nitride, tungsten nitride, or tungsten silicon nitride (not shown in FIG. 1).

For aluminum as well as copper chip metallization, the insulator under the metallization is typically silicon dioxide. However, with the recent trend towards dielectric materials of lower dielectric constants, films made of silicon-containing hydrogen silsesquioxane (HSQ), aerogels, organic polyimides and parylenes are also used in spite of the fact that they are less dense and mechanically weaker than previous standard insulators such as the plasma-enhanced chemical vapor deposited dielectrics. Also, stacks of dielectric layers may be used such as alternating layers of plasma-generated tetraethylorthosilicate (TEOS) oxide and HSQ, or ozone TEOS oxide and HSQ.

In order to strengthen the chip contact pad mechanically, reinforcing structures are sometimes placed under the bonding pad (not shown in FIG. 1). Descriptions may be found in U.S. Patents # 6,1443,396, issued 11/07/2000 (Saran et al., System and Method for Reinforcing a Bond Pad), and # 6,232,662, issued 05/15/2001 (Saran, System and Method for Bonding over Active Integrated Circuits), and U.S. Patent Application # 09/312,385, filed 05/14/1999 (Saran et al., "Fine Pitch System and Method for Reinforcing Bond Pads in Semiconductor Devices").

In the embodiment of FIG. 1, the contact pad has an added conductive layer 105 on the pad metallization 103. This layer 105 is conformal to the surface of the chip and provides a reliable, low resistance contact to the pad metallization 103. As FIG. 1 shows, layer 105 covers not only the area of the pad 102b proper, but also the window side walls of protective layers 104 and a portion of the

surface surrounding the pad window. The preferred material for layer 105 is a so-called under-bump metallization, which has been investigated in numerous literature publications. For instance, reliability risks, as well as
5 the requirements for special pad metallizations, have been described in a series of detailed publications by the International Business Machines Corporation in 1969 (IBM J. Res. Develop., Vol. 13, pp. 226 - 296): P. A. Totta et al., SLT Device Metallurgy and its Monolithic Extension, L. F.
10 Miller, Controlled Collapse Reflow Chip Joining, L.S. Goldmann, Geometric Optimization of Controlled Collapse Interconnections, K. C. Norris et al., Reliability of Controlled Collapse Interconnections, S. Oktay, Parametric Study of Temperature Profiles in Chips Joined by Controlled
15 Collapse Techniques, B. S. Berry et al., Studies of the SLT Chip Terminal Metallurgy.

The I/O pads 102 in FIG. 1 have a metallization 105 suitable for attachment to outside parts either by forming

- welds under thermocompression bonding, or
- 20 • solder connections under reflow conditions (using solder material 107, preferably solder "balls", or
- adhesive connections under adhesive attachment (using electrically conductive adhesives).

An important feature of the present invention is
25 protective plastic film 106 of controlled and uniform thickness, which is selectively attached to passive chip surface 101b. Suitable films are commercially available; examples include NEX-130C from Nippon Steel, Japan; CNB-768-35 from Dexter, USA; CEL-C-4100F from Hitachi, Japan;
30 and CEL-C-7240 from Hitachi, Japan. The films are selected from a group of electrically insulating materials including

polyimide, epoxy resin, and silicone. These films are adhesive only on one side, namely the side to be attached to the passive semiconductor chip surface. The film thickness ranges usually from 20 to 60 μm , with preferred
5 thicknesses being 25 μm and 50 μm .

The most outstanding film characteristic is its light absorbing capability in the visible and infrared wavelengths regimes. Furthermore, the film remains insensitive to moisture absorption, and exerts
10 thermomechanical stress on the chip such that this stress at least partially neutralizes the stress exerted by an outside part (such as a printed circuit board) after chip assembly.

As examples, some characteristics of the films LE-5000X of Lintec, and NEX-930L of Nippon Steel are tabulated
15 in TABLE 1.

TABLE 1

| | LE-5000X | | NEX-930L |
|------------|------------------|------------------|------------------|
| | 25 μm | 50 μm | 50 μm |
| Thickness | 25 μm | 50 μm | 50 μm |
| Filler | No | Yes (70%) | Yes (70%) |
| Color | Black/Blue | Black | Black |
| Carbon % | 1.3/0.65 | 1.3/0.65 | 0.34/0.73 |
| 25 Warpage | Good | Good | Good |
| Dicing | Good | Good | Good |

As an example for the light absorption, FIG. 2 plots the light transmission data (in %) measured as a function
30 of light wavelength (in nm) for the Lintec LE-5000X for the thickness of 50 μm . As the plot shows, the light penetration ratio is less than 4 % for all samples.

Similarly, FIG. 3 plots the light transmission data (in %) measured as a function of light wavelength (in nm) for the Nippon Steel film NEX-930L in the thicknesses of 50 and 100 μm . As the plot shows, the light penetration ratio is less than 1 % for all samples, and differences between filler or carbon contents of the film variations are minimal and barely distinguishable on the scale of the plot.

It is a technical advantage of the present invention that the neutralizing stress provided by the film can be achieved by a film selected for two suitable parameters: thickness, and coefficient of thermal expansion (CTE). Preferably, the film CTE is approximately matching the CTE of the outside part, such as a printed wiring board. A preferred range of CTE is about 18 to 45 ppm/ $^{\circ}\text{C}$, coupled with a flexural modulus of about 16 to 19 GPa. Examples of suitable film characteristics, offered by several film manufacturers, are listed in TABLE 2.

TABLE 2

| | (Star Film) | | | |
|--------------------|--------------|-----------|-----------------|-----------------|
| | Nippon Steel | Dexter | Hitachi | Hitachi |
| | NEX-130C | CNB768-35 | CEL-C-4100F | CEL-C-7240 |
| Density (g/cc) | 1.77 | | | |
| Tg (C) | 165 | 145-170 | 64 | 96 |
| Ef (GPa) | 16 | | 0.9 | 19.4 |
| Flex Str (MPa) | 130 | | | |
| a1 (ppm/C) | 19 | 11 | 130 | 12 |
| a2 (ppm/C) | 45 | 20 | | 42 |
| Vol. Res. (ohm*cm) | 5.00E+16 | | | |
| Water Abs. (%) | 0.85 | | 0.5 | 0.35 |
| Cl- (ppm) | 70 | | 4.3 | 1.1 |
| Na+ (ppm) | 3 | | 1.5 | 0.9 |
| Pot life (hr) | N/A | | 24 | 8 |
| Cure (C*hr) | | 165*0.5 | 120*1+ 150*3 | 130*1+ 180*3 |

5 The effect of film 106 in FIG. 1 to reduce stress on the joints of the I/O pads with the outside part can be supported by the configuration of the I/O pads. (The stress reduction can be achieved whether the joint is by direct contact with metallization 105, or solder balls 107

10 are used). The I/O pads on the active chip surface should preferably be configured in proximity to the stress-neutral central chip portion and distant from the stress-maximum peripheral chip portions. The pad positioning in the stress-neutral central chip portion minimizes any stress

15 caused by the CTE difference of an outside part, such as a printed wiring board made of materials like FR-4, FR-5 and

BT resin (with or without strengthening or thermally modulating fibers), relative to the CTE of silicon. The stress-mitigating influence of film 106 can thus become particularly pronounced. If possible, the CTE of the outside part should be selected to be approximately matching the CTE of plastic film 106.

In order to give a more detailed example, the film material NEX-130C, commercially offered by Nippon Steel Chemical Co., Japan, is listed in TABLE 3. Notable among the film parameters is an adhesion strength to the passive chip surface of about 400 kg/cm² after curing, and a moisture absorption of about 0.85 weight % without changing any film properties.

TABLE 3

| ITEM | UNIT | STANDARD | TOLERANCE |
|---|--------------------|----------|-----------|
| -Working Properties | | | |
| Viscosity @ 150 deg.C | Poise | 350 | +--150 |
| Cure Time @ 180 deg.C | sec. | 160 | +--30 |
| -Physical Properties | | | |
| Specific Gravity | | 1.77 | +--0.05 |
| Thermal Expansion, Alpha-1 | ppm | 19 | +--5 |
| Thermal Expansion, Alpha-2 | ppm | 45 | +--15 |
| Glass Transition Temperature | Deg. C | 165 | +--15 |
| Flexural Strength | MPa | 130 | +--40 |
| Flexural Modulus | MPa | 16000 | +--2000 |
| Heat Conductivity | W/mK | 0.6 | +--0.1 |
| Water Absorption | wt% | 0.85 | +--0.15 |
| Adhesion Strength, Cured @ 150 deg.C, 1 hr. | kg/cm ² | 400 | +--150 |
| Heat Decomposition Temp. | deg. C | 340 | +--25 |
| -Electric Properties | | | |
| Volume Resistance | ohm*cm | 5E+16 | +--4E+16 |
| Dielectric Constant | | 3.7 | +--0.3 |
| Dielectric Loss | | 0.010 | +--0.002 |
| -Chemical Properties | | | |
| Ionic Chloride Content | ppm | 70 | +--70 |
| Ionic Sodium Content | ppm | 3 | +--3 |
| -Working Properties (Reference) | | | |
| Provisional Adhesive Strength* ¹ | kg/cm ² | min. 5 | |

*1) "Provisional Adhesive Strength" is a new determination item.

Further detail about the raw material components of the selected example material NEX-130C is tabulated in TABLE 4. Especially noteworthy is the content of

about 4 % amine type hardener; about 5 % thermoplastic resin tackyfier; and fillers of two kinds, about 50 to 60 % larger particle size silica, and about 12 to 15 % smaller particle size silica.

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TABLE 4

| Entity | Name of Raw Material | Percentage |
|-------------------|------------------------------|------------|
| 10 Epoxy resin | Solid epoxy resin | 15.2 % |
| | Liquid epoxy resin | 5.1 % |
| Hardener | Amine type | 4.0 % |
| Catalyst | Imidazol type | 0.4 % |
| Tackyfier | Thermo plastic resin | 5.1 % |
| 15 Coupling agent | Epôxy silane | 0.5 % |
| Additive | Silicone intermediate | 0.3 % |
| Fillers | Larger particle size silica | 55.5 % |
| | Smaller particle size silica | 13.9 % |
| | Total | 100.0 % |

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It should be noted that the percentages quoted are variable; they are intended to indicate value ranges rather than fixed numbers.

As another characteristic, it is advantageous that the film, after curing, can be clearly marked by a laser for inscribing information such as product type, manufacturer, date, origin etc.; the above quoted example material NEX-130C has this characteristic.

FIGs. 4A, 4B, 5A, 5B, 6 and 7 illustrate in simplified manner the process flow for completing the fabrication of a semiconductor device according to the invention.

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- FIG. 4A: Providing a semiconductor wafer 401 having an active surface (not shown in FIG. 4A) and a passive surface 402; the active surface includes a plurality of chips having I/Cs and I/O pads suitable for metallurgical contacts;
- FIG. 4B: providing a suitable length of adhesive plastic film 403 of controlled and uniform thickness, this film suitable to absorb light of visible and infrared wavelengths, to remain insensitive to moisture absorption, and to exert thermomechanical stress on the chips such that the stress at least partially neutralizes the stress exerted by an outside part after chip assembly. Film 403 is provided from a large roll 501, as depicted in FIG. 5A. Since the film 502 is adhesive on one of its surfaces, it is supplied with cover sheets 503 and 504 on its two surfaces, respectively.
- FIG. 6: rolling the film 403 onto the passive wafer Surface 402;
- FIG. 7: curing the film 403 at elevated temperatures for a length of time sufficient to increase the adhesion strength between film 403 and the wafer 401 to a predetermined value; preferably, the curing temperature is about 150 °C, and the length of time about 1.0 hr.; and
- singulating the chips of the wafer by sawing the wafer 401 through the semiconductor as well as through the adhering film 403 (step of singulation not shown in FIG. 7).

While this invention has been described in reference to illustrative embodiments, this description is not

intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon
5 reference to the description.

It is therefore intended that the appended claims encompass any such modifications or embodiments.